## REMARKS

No amendments, cancellations or additions have been made to the claims of the presently claimed case. As such, claims 1-13, 17-21, and 23-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

**Section 103 Rejections**

Claims 1-11, 17-19, and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,862,242 to Wildi et al. (hereinafter "Wildi") in view of U.S. Patent No. 4,799,098 to Ikeda et al. (hereinafter "Ikeda"). In addition, claims 12, 13, 20, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wildi in view of U.S Patent No. 6,051,868 to Watanabe et al. (hereinafter "Watanabe"). As will be set forth in more detail below, the § 103 rejections of claims 1-13, 17-21, and 23-25 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); and, MPEP 2143.01. The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

**None of the cited art teaches or suggests, or can be combined or modified to teach or suggest, an integrated circuit with a buried layer of opposite conductivity than a well region formed above the buried layer, where the buried layer includes a first portion underlying a transistor formed within the well region and a second portion spaced apart from and laterally surrounding the first portion.** Independent claim 1 recites in part: "a buried layer formed within a substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region, and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion." As noted in the Office Action, "Wildi fails to disclose ... a buried layer include[ing] a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion." (Office Action -- page 2). In an attempt to overcome the

deficiencies of Wildi, the Office Action cites Ikeda as disclosing "... a buried layer with various portions (2, 2', 14, 14') ..." and suggests "... it would have been obvious to one having ordinary skill in the art ... to modify the semiconductor device of Wildi to include a buried layer with various portions as disclosed in Ikeda because it aids in increasing the speed of the device ..." (Office Action -- page 2-3). Such a citing of Ikeda and the suggestion to combine the teachings of Ikeda and Wildi, however, are traversed.

In particular, it is asserted that Ikeda does not teach or suggest a buried layer with a first portion and a second portion spaced apart and laterally surrounding the first portion. Rather, Ikeda teaches a plurality of separate and distinct buried layers formed to provide benefits to different respective features of the device. For example, Ikeda teaches the inclusion of n-type buried layer 2 to control the punch-through voltage of an overlying PMOS transistor, thereby distinguishing n-type buried layer 2 to be separate and distinct from n-type buried layer 2' formed beneath the bipolar transistor. In addition, Ikeda teaches p-type buried layer 14' formed underneath a device isolation region to allow for an increased integration density across the wafer. P-type buried layer 14, on the other hand, serves to reduce the resistance of well region 5 of the NMOS transistor. Consequently, none of buried layers 2, 2', 14, and 14' are portions of one buried layer as suggested in the Office Action. In addition, there is no teaching or suggestion within Ikeda that any of buried layers 2, 2', 14, and 14' are annular structures. As such, there is no teaching or suggestion that any of buried layers 2, 2', 14, and 14' are spaced apart from and laterally surrounding another of the buried layers. Consequently, Ikeda does not teach or suggest the limitations of claim 1. Since neither Ikeda nor Wildi teach or suggest a buried layer including a first portion and a second portion spaced apart from and laterally surrounding the first portion, no combination of Ikeda or Wildi can teach or suggest a buried layer with such a limitation. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03.

Even if Ikeda taught or suggested a buried layer with a first portion and a second portion spaced apart from and laterally surrounding the first portion, there is no motivation to combine Ikeda with Wildi to teach all of the limitations of claim 1. For instance, Wildi specifically teaches a buried layer of opposite conductivity than the substrate and an overlying well region such that a device formed within the well region may be electrically isolated from the substrate. In contrast, Ikeda specifically discloses a buried layer with the same conductivity as an overlying well such that the electrical resistance of the well region may be decreased. In particular, Ikeda teaches an NMOS transistor formed within p-type well 5 and having p-type buried layer 14 underneath. Such a configuration, however, does not electrically isolate the

NMOS transistor from other devices within the circuit as necessitated by objective of Wildi. As such, there is no motivation to combine the teachings of Wildi and Ikeda to create a buried layer including a first portion and a second portion spaced apart from and laterally surrounding the first portion, wherein the buried layer comprises the opposite conductivity type of the substrate and an overlying well region as recited in claim 1. More specifically, there is no motivation to modify or combine Wildi and Ikeda to teach the limitations of the presently claimed case.

Furthermore, Watanabe cannot be combined with Wildi and/or Ikeda to overcome the deficiencies therein. As noted in a response to a previous Office Action mailed August 14, 2002, Watanabe does not teach or suggest an integrated circuit with a buried layer of opposite conductivity type than an overlying well region. Furthermore, Watanabe does not provide any motivation to create an integrated circuit with such a limitation, since Watanabe specifically teaches that cross talk is undesirably generated by parasitic capacitance between layers of opposite conductivity type. Consequently, there is no motivation to combine Watanabe with Wildi and/or Ikeda to teach the limitations of claim 1.

**None of the cited art teaches or suggests a doped annular region extending through a well region.** Independent claim 17 recites in part: "[a]n integrated circuit, comprising ... a doped annular region extending through the well region to contact the buried layer...". Neither Wildi, Ikeda nor Watanabe teach or suggest having a doped annular region extending through a well region. In particular, Ikeda fails to disclose any doped region extending through p-type well 5, much less a doped annular region through such a well region. In addition, Watanabe fails to disclose a well region below bipolar transistors 108 and 109 and, therefore, cannot teach or suggest a doped annular region extending through a well region. Although Wildi does teach high voltage region 316 surrounding transistor 350 and having the same conductivity type as buried layer 318, high voltage region 316 does not extend through well region 351. As such, Wildi does not teach or suggest a device within a doped annular region extending through a well region as recited in claim 17. Since none of the cited art teaches or suggests a doped annular region extending through a well region, no combination of the cited art can teach or suggest a buried layer with such a limitation. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03.

For at least the reasons set forth above, none of the cited art, either individually or in combination, teaches, suggests, or provides motivation for all limitations of independent claims 1 and 17. Therefore, independent claim 1 and 17, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of the § 103(a) rejection of claims 1-13, 17-21, and 23-25. In addition to being patentable for reasons set forth above, several of the dependent claims are believed to be separately patentable for reasons set forth below.

For example, claims 4 and 5 specify the distance between the first and second portions of the buried layer as recited in claim 1 as being less than about 5 microns and approximately 1.2 microns, respectively. The Office Action admittedly states that Wildi fails to disclose the limitations of claims 4 and 5. The Office Action further states that "... the applicant has not established the critical nature of the dimension of less than 5 microns..." and "... approximately 1.2 microns." Such statements are traversed, however, since the Specification clearly teaches the criticality of fabricating buried layer portions with such separation distances. In particular, the Specification states:

> The spacing needed between two such openings in the masking layer depends on the final separation of the buried layer portions desired, allowing for diffusion during processing. The final desired separation in turn depends on details, such as doping levels, of the particular fabrication process used. In some embodiments, for example, a masking layer spacing of about 2.1 microns may result in a post-processing separation of about 1.2 microns between the buried layer portions. In an embodiment, the separation between the buried layer portions after processing is such that the oppositely-doped region between the portions is "pinched off" during operation by depletion regions at the lower end of the buried layer, while retaining some undepleted material at the upper end of the buried layer. Such an embodiment is illustrated using dashed-line depletion region boundaries 90 in Fig. 8. The buried layer may separation be designed so that the "pinch-off" occurs when outer buried layer portion 88 is connected to VCC (for an n+ buried layer). This "pinch-off" may reduce substantially the coupling of noise generated by n-channel transistor 63 to p-type substrate 46. (Specification – page 15, lines 16-29)

As such, it is asserted that the Applicant has established the critical nature of the dimensions specified in claims 4 and 5.

In addition, the cited art fails to even teach or suggest the inclusion of a depletion region between the first and second portions of the buried layer as recited in claim 1. As such, none of the cited art can teach or suggest the limitations of claim 23-25. Accordingly, claims 23-25 are asserted to be patentably distinct over the cited art.

With regard to claim 8, the cited art fails to provide an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor. As such, claim 8 is asserted to be patentably distinct over the cited art.

The Office Action suggests the term 'adapted to' in claims 10 and 17-19 does not provide a positive limitation by which to further limit the claims. On the contrary, the aforementioned claim terminology is used in the present claims to impart proper functional limitations upon the elements of the claims. In other words, the use of such terminology may define a claim element (e.g. metallization) by what it does, rather than by what it is. Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971), MPEP 2173.05(g). In fact, functional limitations, like any other claim limitations, must be evaluated and considered for what they fairly convey to a person of ordinary skill in the pertinent art. MPEP 2173.05(g). Such an evaluation may be used to show that functional limitations are definite and proper, as illustrated by more recent court decisions.

For example, claim language calling for a sleeve "adapted to be fitted" over an insulating jacket has been ruled to impart structural limitation to the sleeve rather than to merely direct activities which may take place in the future. *In re Venezia*, 189 USPQ 149 (CCPA 1976), MPEP 2173.05(g). The court's opinion states in part: "As we view these claims, they precisely define a group or "kit" of interrelated parts. These interrelated parts may or may not be later assembled to form a completed connector. But what may or may not happen in the future is *not* a part of the claimed invention. The claimed invention does include present structural limitations on each part, which structural limitations are defined by how the parts are to be interconnected in the final assembly, if assembled". The opinion further states: "Again, a present structural configuration for the housing is defined in accordance with how the housing interrelates with the other structures in the completed assembly...More particularly, we find nothing indefinite in these claims. One skilled in the art would have no difficulty in determining whether or not a particular collection of components infringed the collection of interrelated components defined by these claims."

A similar line of reasoning may be properly applied to the functional limitations in the present claims. For example, a limitation on metallization to preclude connection of an doped annular region to the opposite polarity of a supply voltage connected to a well region may facilitate metallization which is configured to provide such a function. For example, the metallization may be configured to connect to a well region of the circuit but not to the doped annular region as recited in claim 18. Alternatively, the

metallization may be configured to connect to the well region and doped annular region to the same polarity as recited in claim 19. In any case, such configurations of the metallization may serve as adaptations of the integrated circuit to achieve the claimed distribution of voltage. Therefore, the 'adapted to' language used within claims 10 and 17-19 does place limitations on the claimed integrated circuits. Consequently, the limitations of claims 10 and 17-19 are asserted to be patentable.

## CONCLUSION

This response constitutes a complete response to all of the issues raised in the Office Action mailed January 31, 2003. In view of the remarks traversing rejections, Applicants assert that pending claims 1-13, 17-21, and 23-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-04500.

Respectfully submitted,

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